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Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

Dean et al.

For: **TEST SYSTEM FOR INTEGRATED CIRCUITS**

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL046031154US**
- ☒ **seven (7)** sheets of drawings.
- ☐ A certified copy of a application.
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APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAME: Alvar A. Dean and Sebastian T. Ventrone

TITLE: TEST SYSTEM FOR INTEGRATED CIRCUITS

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INTERNATIONAL BUSINESS MACHINES CORPORATION

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TEST SYSTEM FOR INTEGRATED CIRCUITS

Field of the Invention

The present invention is generally related to testing systems for integrated circuits. It is also related to systems for parallel testing integrated circuit chips. It is more specifically related to an in-transit test system for testing application specific integrated circuits (ASICs).

Description of the Related Art

Application specific integrated circuits (ASICs) are customized circuits which are generally produced in limited numbers. Testing such circuits present problems because of the unique role each different ASIC batch is designed to perform.

More specifically, the design for an ASIC is usually supplied to a semiconductor foundry which manufactures individual chip packages. The chip packages are then to shipped to a different location such as a module build house, which packages the chips. The packaged chips are then shipped to a different location, usually back to the original foundry, to be tested. After being tested the non-defective chips are shipped to a different location such as the system house for system assembly.

The extra processing required to test the ASIC adds substantially to the cost of the product being produced and increases the time that it takes to bring a product to market. Further, conventional testing mechanisms generally comprise large multi-million dollar testing operations which are capable of performing the varied testing that the uniquely

functioning ASICs require. Therefore, there is a need to reduce the time and resources devoted to testing ASIC products.

Summary of the Invention

It is therefore an object of the present invention to provide a scheme for testing a plurality of integrated circuits at one time.

It is another object of the present invention to provide test stimuli in parallel to a plurality of chips circuits and to compare outputs of all chips in a single step as an indication of passing or failing.

It is yet another object of the present invention to distinguish passing and failing chips by comparing chip output data with data from a golden chip.

These and other objects of the invention are accomplished with a tester for testing a plurality of chips that comprises a test control device. The test control device turns on at least one test engine to provide test signal to the plurality of chips in parallel. A checking circuit compares output signal of the plurality of chips with each other. A golden output signal is used to replace defective output signal from a failing chip. The circuit is located local to said chips.

A control device verifies the functionality of each chip and records passing or failing chips. In one embodiment, the test control device operates while the tester is in transit. The checking circuit compares all the chips with each other. The tester also includes a visible indicator showing the passing or failing chips. The visible indicator could be a light or a register.

The chips are tested simultaneously and the outputs of the chips are compared to each other. Sockets for holding and contacting the chips, the test control device, the test engine, and the checking circuit can all be on a single card. Multiple cards can also be used. The test engine includes a BIST engine or read only memory with stored test patterns.

Another embodiment of the invention is a device for transporting integrated circuit chips that includes a test circuit connected to the integrated circuit chips. The test circuit tests the integrated circuit chips during transport. The device includes a power supply connected to the test circuit and an indicator for identifying which ones of the integrated circuit chips failed the testing. The indicator could be a memory such as a register or an LED. The test circuit includes a control device and connections between the control device and the integrated circuit chips.

Yet another embodiment of the invention is a method for testing integrated circuit chips which includes transporting the integrated circuit chips, testing the integrated circuit chips, supplying power to a test circuit connected to the integrated circuit chips during the transporting, and identifying which ones of the integrated circuit chips failed the testing. The identifying includes storing results of the testing in a memory or illuminating a light. The testing includes connecting the integrated circuit chips to a test circuit within a transportation device.

Yet another embodiment of the invention is a method of testing an integrated circuit chip. The method includes the steps of providing a golden chip; providing test patterns for testing the chip under test and for testing the golden chip; and comparing an output signal from the chip under test with an output signal from the golden chip to determine whether the chip under test passes or fails.

The invention provides a substantially simplified system for testing ASIC chips because the invention does not need to know the output a given input should produce. This is especially important in ASIC chip testing because each different design of ASIC chips has a potentially different output for a given input. Further, since the invention tests the chips during transit, the testing time does not add to the manufacturing time (assuming that the transportation time is longer than the testing time). Thus, the invention helps speed ASIC chip products to market by simplifying the testing process (and thereby reducing testing time) and by performing the testing during transit to further reduce overall processing time.

In addition, the invention saves test time by providing parallel testing of chips at wafer-test or at module test within the factory.

Brief Description of the Drawings

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of preferred embodiments of the invention with reference to the drawings, in which:

FIG. 1 is a schematic diagram of a test box comprising test boards of the present invention;

FIG. 2 is a schematic diagram of an in-transit box;

FIG. 3 is a schematic diagram of a test board;

FIG. 4a is a schematic diagram of a chip testing arrangement including more details of the embodiment illustrated in FIG. 3;

FIG. 4b is a schematic diagram of a the checker/comparator circuit of FIG. 4a;

FIG. 5 is a schematic diagram of an alternated embodiment of the chip testing arrangement of FIG. 3;

FIG. 6 is a flowchart representation of the invention; and

FIG. 7 is a schematic diagram of an alternate chip testing arrangement wherein outputs of all chips are simultaneously compared with outputs of a golden chip;

Detailed Description of the Invention

The invention includes the ability to test products while in transit. Test box 10 is shown in FIG. 1, including a plurality of test boards 11 connected to power supply bus 12 which is powered by a battery 13 or alternatively connected to an external power source by power leads 14.

In-transit box 20 that includes multiple test boxes 10 as shown in FIG. 2. FIG. 2 also illustrates in-transit power bus 21 and power leads 14 supplying power to each individual test box 10 that are included in in-transit test box 20. A primary function of test box 10 and in-transit box 20 is to supply power to test boards 11 so that testing can occur during transit, thereby avoiding increasing manufacturing time for testing.

Test board 11 is illustrated in greater detail in FIG. 3. More specifically, test

board 11 includes sockets into which chips 30 are inserted and control device 31 connected to each of the circuits through lines 32, 33. Chips 30 are typically packaged integrated circuit chips which can be inserted into sockets for providing electrical connection. Control device 31 is shown in more detail in FIG. 4, and includes output MUX 40, checker/comparator 41, test control register 46, test control register mask (TCR) 48, and status indicator 44. While a limited number of chips30 and sockets are shown in FIG. 3, test board 11 could include any number of chip 30 and sockets.

Control device 31 tests all chips 30 connected to test board 11 by applying a signal on line 39 to test stimuli generator 34 which sends the test pattern on lines 32 to the inputs of all chips 30 in parallel. Chips 30 return output signals to control device 31 along individual lines from each chip output that make up line 33. Thus, if each chip has m outputs, line 33 includes m individual lines from each chip. If there are n chips, line 33 includes m x n individual lines. Control device 31 groups signals from each output from all chips and compares these groups of signals in parallel (FIG. 4b). If all return signals from corresponding chip output pins are identical, control device 31 reports a pass for that test stimuli and sends a signal to test stimuli generator 34 to send out the next test pattern. When control device 31 detects a difference from the individual lines in output line 33 from each chip 30 then it sets a fail condition in control device 31. It then proceeds to determine which chip is bad. Once determined as a bad chip, the chip is labeled as defective and removed from further testing.

More specifically, in FIG. 3, during the test, each chip under test 30 is supplied with test stimuli from test stimuli generator 34 along signal lines 32, as shown in FIG. 3. Test stimuli generator 34 can be a BIST engine and/or it can be test patterns supplied from a memory source, such as a RAM or a ROM. As a result of the test stimuli, each chip under test will respond on its own individual output lines. The lines from all chips

are designated in FIG. 3 as output line 33 which carry test results from corresponding outputs of all chips to controller 31. If every chip is good, then each set of individual lines from corresponding outputs of each chip in output line 33 will have identical values. Control device 31 doing the comparison would find all good chips. If some chips are bad, some values on a line in output line 33 would be different from other signals from corresponding outputs of other chips that arrive in parallel.

In one embodiment, visual indicator 35 is provided for each chip 30, which is connected to the control device 31 by line 36, to indicate to the operator which chips passed and which chips failed during the testing process. Visual indicator 35 can be a light emitting diode (LED), for example. The defective chips could be discarded or returned to the previous processing area (e.g., left on the test board) for evaluation.

FIG. 4 illustrates more details about test stimuli generator 34 and control device 31 in FIG. 3. Test stimuli generator 34 is a source of test patterns, such as built in self test (BIST) engine 42 and seed patterns 43. Control device 31 includes MUX 40, exclusive NOR (XNOR) checker/comparator 41, golden chip 37, test control register (TCR) mask 48, and status indicator 44. BIST engine 42 uses the seed patterns 43 to produce the test stimuli. The number of XNOR checker/comparators 41a to 41m, is equal to the number of outputs m each chip has, as shown in FIG. 4b. Each XNOR checker/comparator 41a-41m, is n-way, where n is the number of sockets for holding chips to be tested.

Seed pattern 43 can be stored in ROM or generated by a logic circuit. The output from BIST engine 42 is supplied to each of the chips 30 via input line 32. Outputs "a" from all n chips 30 extend through MUX 40a to 40n to XNOR 41a (FIG. 4b) of XNOR 41 along individual lines 33a to 33n of line 33. Signals along these n lines are checked for matching in XNOR 41a. Checker comparator 41 includes all the XNOR gates for

corresponding output lines from each chip in line 33 plus an OR gate that passes through any defect information from any of these XNOR outputs, as shown in FIG. 4b. The output of checker comparator 41 would be an off state, i.e. zero, if all corresponding outputs on line 33 are the same. If one or more outputs differ, then the output of checker comparator 41 on line 45 is reversed, and goes to an on state, i.e. 1. Thus, the presence of a single defect in data from one output on one chip is determined by the presence of a 1 on line 45.

If output line 45 indicates a fail, then test board 11 includes one or more bad chips. To determine which of chips 30a to 30n being tested is defective, the following process is used to isolate a bad chip or bad chips and to replace data from that bad chip with known good data from golden chip 37.

Test control register 46 switches MUX 40a to turn off signal from chip 30a of the array of chips 30. The signal to checker/comparator 41 from chip 30a is replaced with signal to MUX 40a from golden chip 37 that is provided along line 54 under the control of select line 47 from test control register 46. Since golden chip 37 is guaranteed to provide a passing test result, MUX 40a will certainly now generate a passing result. If chip 30a was the only defective chip, then all inputs to checker/comparator 41 will now match and line 45 will report a 0 or pass. In that case, chip 30a has been identified as the failing chip; it is permanently replaced by golden chip 37 and marked by status indicator 44 and TCR mask 48 as being a bad chip. If line 45 does not go to a pass, then the test control register 46 then switches MUX 40a and MUX 40b to turn off signal from chips 30a and 30b of the array of chips 30 and to replace their data with data from golden chip 37. Data to each MUX 40a to 40n is sequentially replaced with data from golden chip 37 and the test results are re-sampled until output line 45 goes to a pass status. The last MUX, for example MUX 40e, which is turned off before the pass status is achieved must

have been connected to a defective chip, in this case chip 30e. Once failing chip 30e has been detected a register bit corresponding to defective chip 30e in TCR mask 48 is turned on to permanently identify chip 30e as failing. This register bit permanently replaces signal to its MUX 40e from that failing chip 30e with signal from golden chip 37 and permanently sets the status indicator for chip 30e as a fail.

The system allows identification of more than one failing chip. Once the last failing chip has been isolated, line 45 will show passing as described above. Now all previously good isolated chips 30 (those not previously identified as failing in the TCR mask) are reenabled by their corresponding output MUX 40 as controlled by line 47 from test control register 46. The process is repeated to determine whether other chips 30 are failing for the current test stimuli and to identify those chips.

The TCR mask 48 and status indicator 44 are written to keep MUX 40 of a defective chip connected to golden chip 37 through line 49. TCR 46 permanently selects golden chip data through that MUX 40 that was connected to the defective chip for the remaining portion of the test using output line 49 from TCR mask 48. From that point on, TCR mask 48 locks the status bit of the defective chip in the status indicator 44. In this manner, as each failing chip is identified, it is isolated, marked, removed from any further testing, and its data replaced by data from golden chip 37.

Thus, while the test is underway, test control register 46 enables MUX 40 with an individual control signal along control signal bus 47 for each of the n chips under test. In this manner, test control register 46 allows the output signals from all chips to propagate to checker/comparator 41 to compare signals with all other test chips. If all the chips pass, meaning that all their corresponding outputs are at the same logic value, the output of the checker 41 would be "pass."

The test results are stored in status indicator 44, which may be a simple array of LEDs or a memory chip which can be queried electronically at the system house. Thus, as with the structure shown in FIG. 3, a visual indicator could identify the defective chips or status indicator 44 could be downloaded to a test computer. The test computer could read onboard status indicator 44 to download the results of the in-transit testing. The good chips would go onto the next stage of assembly, while the bad chips would be discarded or sent back to the chip provider.

In an alternate embodiment, each XNOR checker/comparator 41, is n+1-way, where n is the number of sockets for holding chips to be tested, and the additional input to XNOR checker/comparator 41 comes from golden chip 37. This allows identification of a defect on line 45 even if all chips (except golden chip 37) are defective in exactly the same way.

Additional features that can be added to test board 11 are illustrated in FIG. 5. Instructions stored in memory 50 such as a clock signal or test patterns, etc. are supplied to the chips 30 in addition to (or as an alternative to) patterns from BIST engine 42. Memory 50 can be a RAM, a ROM, or any other storage medium. For example, the product under test may be a microprocessor, and specific product application code stored in memory 50 can be run in addition to patterns generated by BIST engine 42.

During high speed testing, output of all chips 30 can be stored in memory 53. High speed testing is preferably done one chip at a time but can be done in parallel. At any time, test control register 46 could check memory 53 using comparator 57 to compare test data stored in memory 53 with golden data stored in golden pattern memory 58. Golden data in golden pattern memory 58 was generated from previous controlled experimental testing, from simulation, or directly from golden chip 37 during testing. If

the contents of memory 53 are different than the contents of golden memory 58, the process described above using golden chip 37 is used to determine which chip is defective. Once a failing chip is isolated, it is removed from further testing, and marked as a fail.

In addition to providing for testing during transport, the invention saves test time by providing parallel testing of chips at wafer-test or at module test within the factory. For wafer test, a test fixture, such as those known in the art for multi-die testing or for wafer-level burn-in, can be provided that contacts a large number of chips or all chips on the wafer simultaneously. The circuit described herein above is provided locally to the wafer on that test fixture or wafer interface board. Thus, by providing the golden signal for compare local to the chips being tested the number of tester channels needed for multiple chip testing is sharply reduced. Preferably that golden output signal is provided by a golden chip running simultaneously with the chips under test. It can also be provided from memory connected to the wafer or module test board. By providing a local compare all outputs of each chip can be measured, a significant advantage over testers that reduce pin count to each chip to limit the number of tester channels.

FIG. 6 is a flowchart illustrating an embodiment of the invention. Block 60 represents the start of the process. The status indicator is initialized to indicate that all chips are good in block 61. Test patterns from test stimuli generator 34, RAM 50 and/or BIST engine 42 are applied to chips 30 in block 62. Checker/comparator 41 monitors the signal returned from test chips 30 and defects found on line 45 are noted in status indicator 44, as shown in block 62. Whether all chips passed or not, the state of line 45 is determined in block 63. If they did not all pass, the failing chip is isolated and its data is replaced by data from golden chip 37 by sequentially replacing connection in MUX 40 from its chip with connection to golden chip 37, as shown in block 64. As each MUX is

disconnected from its chip, and the defective signal continues to be present, block 65 will return the process to isolate the next chip by sequentially disconnecting connection in the next MUX to its chip, as shown in the no response to block 65. When disconnecting MUX 40 from its chip finally produces a passing signal, the status indicator 44, TCR mask 48, and/or LED 35 record the previously isolated chip as defective, as shown in item 66. All other isolated chips are then turned on again in block 69 and the process resumes at block 62 with application of patterns and monitoring of pass/fail line 45. If all chips are now good, in block 63, whether or not additional test patterns should be applied is determined in block 67. If so, they are applied in block 62. If not processing is completed, and the flowchart terminates at block 68.

As mentioned above, each batch of ASIC chips has potentially different performance parameters from other batches of ASIC chips. This presents special testing problems to conventional systems, because the proper output for each different batch of ASIC chips must be known before the chips can be properly tested. However, with the invention since the chips are merely tested against other chips in the same batch to determine if similar output signals are produced, the invention does not need to know the specific output a given input should produce. This is true whether the chips are tested against other untested neighboring chips or also tested against a known good "golden" chip.

In an alternate embodiment, all chips under test 30 and golden chip 37 are simultaneously provided with the test signal along line 32 as shown in FIG. 7. For each chip under test 30 all m output signals are simultaneously compared with m corresponding output signals of golden chip 37. An array of m 2-way XNOR comparators 70 is used for the comparison for each of the n chips. The m outputs of the comparators 70 for each chip are combined in OR gate 72 to determine whether any output of chip 30

failed the test. If so that chip is identified as a fail by setting TCR mask 48, as described herein above. If a chip is identified as a fail in any test, the TCR mask is not reset in subsequent testing and remains a fail. A similar scheme can be used at wafer test.

The invention allows testing to be performed during transportation by using test box 10 and self-powered in-transit box 20, as discussed above. When a chip is determined to be bad, that information can be maintained in status indicator 44 which can be downloaded and viewed when in-transit box 20 arrives at its location. Alternatively, the chips or test board may provide a visual indication (such as an indicator light 35) of test failure. These test LEDs 35 are placed next to each test chip 30 (FIG.3) and are turned on when a failing chip is identified and removed from further testing. Failing chips would thereby be easily visible.

In operation, after the chips are manufactured in the foundry, they could be mounted on test board 11 and tested during transportation (e.g., on the way to the system house). The chips which were determined to be good, would be removed for assembly, while chips which were determined to be bad could be returned to the foundry (or some other location) in in-transit box 20. This would allow diagnostics to be performed to determine the source of the defect.

Therefore, the invention provides a substantially simplified system for testing ASIC chips by not having to know the output a given input should produce. This is especially important in ASIC chip testing because each different batch of ASIC chips has a potentially different output for a given input. Further, since the invention tests the chips during transit, the testing time does not add to the manufacturing time (assuming that the transportation time is longer than the testing time). Thus, the invention helps speed ASIC chip products to market by simplifying the testing process (and thereby reducing testing

time) and by performing the testing during transit to further reduce overall processing time.

The invention provides the benefit of eliminating chip tests at the receiving site because the parts are tested during the transit stage. Upon unpacking the chips, only fully tested/passing chips would be used for the next phase of card assembly.

Further, with the invention, more test patterns can be applied than would be allowed during the normal manufacturing process. Currently, the test time for each chip cannot be long, since the parts need to be shipped to the customer as soon as possible. However, since testing is now done in transit which can be hours (or even days), more chip test time is available, so many more patterns can be applied and test coverage correspondingly increased. Also different temperature/voltage combinations may be used, so that once the parts reach the final destination, the modules have had far more rigorous testing. This results in higher reliability, reduces in house manufacturing test time and reduces the overall cost by reducing the need for manufacturing testers.

While several embodiments of the invention, together with modifications thereof, have been described in detail herein and illustrated in the accompanying drawings, it will be evident that various further modifications are possible without departing from the scope of the invention. Nothing in the above specification is intended to limit the invention more narrowly than the appended claims. The examples given are intended only to be illustrative rather than exclusive.

What is claimed is:

CLAIMS

1. A tester for testing a plurality of chips, comprising:

a source of test patterns to stimulate the plurality of chips simultaneously;

golden output signal; and

a circuit for simultaneously using outputs of the plurality of chips and said golden output signal to determine which chips pass and which chips fail, wherein said circuit is located local to said chips.

2. The tester as recited in claim 1, further comprising:

a test control device, wherein said test control device controls test patterns for testing said plurality of chips in parallel;

a checking circuit for comparing output signal of said plurality of chips with each other in response to said test patterns; and

wherein said golden output signal is used to replace defective output signal from a failing chip.

3. The tester as recited in claim 2, wherein said test control device controls a test engine.

4. The tester as recited in claim 3, wherein said test engine comprises a BIST engine.

5. The tester as recited in claim 2, wherein said test control device controls a memory with stored patterns.

6. The tester as recited in claim 2, wherein said test control device further comprises a switch for turning off signal from a chip and replacing that signal with said golden output signal.

7. The tester as recited in claim 6, wherein said switch comprises a MUX.

8. The tester as recited in claim 2, further comprising a power supply for providing a power supply voltage, wherein said test control device controls said power supply voltage to provide stress conditions to chips under test.

9. The tester as recited in claim 2, further comprising a temperature control for controlling temperature of the plurality of chips, wherein said test control device controls said temperature to provide stress conditions to chips under test.

10. The tester as recited in claim 2, wherein said checking circuit compares each chip with all other connected chips.

11. The tester as recited in claim 2, wherein said checking circuit comprises an XNOR.

12. The tester as recited in claim 11, wherein said XNOR is at least n-way, where n is the number of chips that can be tested.

13. The tester as recited in claim 12, wherein said XNOR is at least n+1-way, wherein data from a golden chip is always included in data arriving at said XNOR.

14. The tester as recited in claim 2, wherein said golden output signal is provided by a golden chip.

15. The tester as recited in claim 14, further comprising a MUX to isolate a chip and to route signal from said golden chip to replace signal from said isolated chip.

16. The tester as recited in claim 2, further comprising a visible indicator showing passing chips or failing chips.

17. The tester as recited in claim 16, wherein said visible indicator comprises a light.

18. The tester as recited in claim 2, further comprising a register for storing passing or failing chip labels.

19. The tester as recited in claim 2, further comprising sockets for holding the chips, and wherein said sockets, said test control device, said test engine, and said checking circuit are on a single card.

20. The tester as recited in claim 2, further comprising a memory for storing test results for comparison with golden test result data.

21. The tester as recited in claim 2, wherein said golden test result data are provided by a golden chip.

22. The tester as recited in claim 1, wherein said circuit comprises comparing all chip outputs with corresponding golden test result data and then combines results of all comparisons for each chip into a pass or fail signal from each chip.

23. The tester as recited in claim 21, wherein said circuit comprises an array of 2-way XNOR gates and an OR gate for each chip under test.

24. The tester as recited in claim 21, wherein said golden output signal is provided by a golden chip.

25. A device for testing integrated circuit chips comprising a test circuit for connection to a plurality of integrated circuit chips simultaneously, said test circuit for testing said integrated circuit chips during transport.

26. The device in claim 25, wherein said test circuit compares said integrated circuit chips with each other.

27. The device in claim 26, wherein said test circuit compares all said integrated circuit chips with all other integrated circuit chip that have not been found to be defective.

28. The device in claim 25, wherein said test circuit compares all said integrated circuit chips with a golden chip.

29. The device in claim 25, further comprising a power supply connected to said test circuit, wherein said power supply is for providing a power supply voltage to said test circuit and to the chips.

30. The device in claim 29, wherein said test circuit controls said power supply voltage to provide stress conditions to chips under test.

31. The device in claim 25, wherein said test circuit includes a test engine.

32. The device in claim 31, wherein said test engine comprises a BIST circuit.

33. The device in claim 31, wherein said test circuit includes a memory.

34. The device in claim 25, further comprising an indicator for identifying which of the integrated circuit chips failed said testing.

35. The device in claim 34, wherein said indicator comprises a memory.

36. The device in claim 34, wherein said indicator comprises a visual indicator.

37. A method of testing a plurality of integrated circuit chips, comprising the steps of:

a) providing a source of test patterns to stimulate the plurality of chips simultaneously;

b) providing a golden output signal; and

c) providing a circuit for simultaneously using outputs of the plurality of chips and said golden output signal to determine which chips pass and which chips fail, wherein said circuit is located local to said chips.

38. A method of testing as recited in claim 37, wherein in providing step (a) said source of test patterns comprises a BIST engine or a memory.

39. A method of testing as recited in claim 37, further comprising providing a golden chip wherein in providing step (b) said golden output signal comprises output of said golden chip, and wherein in providing step (a) providing said source of test patterns to stimulate said golden chip and the plurality of chips simultaneously.

40. A method of testing as recited in claim 37, wherein in providing step (c) said circuit uses said golden output signal to replace output signal from a chip.

41. A method of testing as recited in claim 37, wherein in providing step (c) said circuit uses said golden output signal to replace output signal from a defective chip.

42. A method of testing as recited in claim 37, wherein in providing step (c) said circuit includes a checking circuit for comparing output signal of said plurality of chips with each other in response to said test patterns.

43. A method of testing as recited in claim 37, wherein in providing step (c) said circuit includes a circuit for comparing output signals of said plurality of chips with said golden output signal to determine whether each of said plurality of chips under test passes or fails.

44. A method of testing as recited in claim 43, wherein in providing step (b) a golden chip provides said golden output signal.

45. A method of testing an integrated circuit chip, comprising the steps of:

a) providing a golden chip;

b) providing test patterns for testing the chip under test and for testing said golden chip; and

c) comparing an output signal from the chip under test with an output signal from said golden chip to determine whether the chip under test passes or fails.

46. The method of testing as recited in claim 45, wherein in providing step (b) said test patterns are provided to a plurality of chips under test simultaneously.

47. A method for testing integrated circuit chips comprising:

a) transporting said integrated circuit chips; and

b) testing said integrated circuit chips during said transporting.

48. The method in claim 47, further comprising supplying power to a test circuit connected to said integrated circuit chips during said transporting.

49. The method in claim 47, further comprising identifying ones of said integrated circuit chips which failed said testing.

50. The method in claim 49, wherein said identifying comprises storing results of said testing in a memory.

51. The method in claim 49, wherein said identifying comprises displaying a visual indicator of passing or failing chips

52. The method in claim 47, wherein said testing includes comparing output signals of said integrated circuit chips with each other.

53. The method in claim 47, wherein said testing includes comparing output signals of one integrated circuit chip with output signals of all other integrated circuit chips that have not been identified as defective.

54. The method in claim 47, wherein said testing includes comparing output signals of said integrated circuit chips with a golden chip.

TEST SYSTEM FOR INTEGRATED CIRCUITS

Abstract

A test board includes a plurality of sockets for connection to a plurality of integrated circuit chips to be tested. A test control device on the board turns on at least one test engine for testing the plurality of chips simultaneously. A checking circuit verifies the functionality of each chip by comparing outputs of chips with each other or with a golden chip. Failing chips are disconnected from further testing and passing or failing chips are recorded.

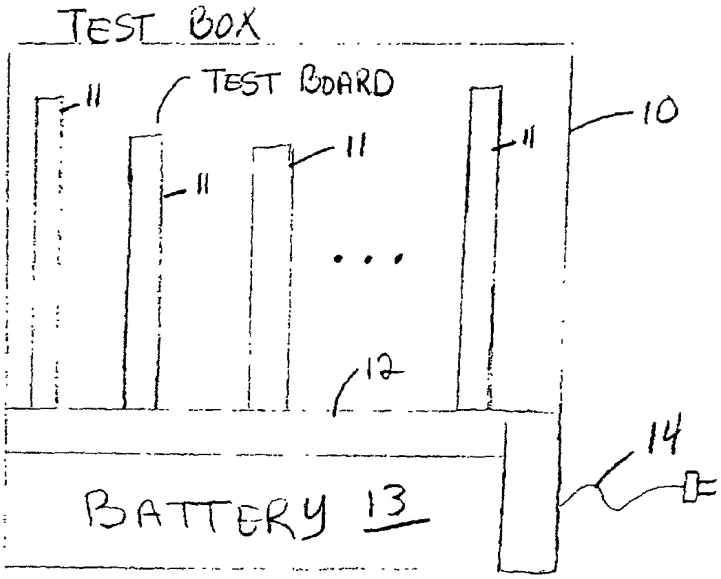

Figure 1

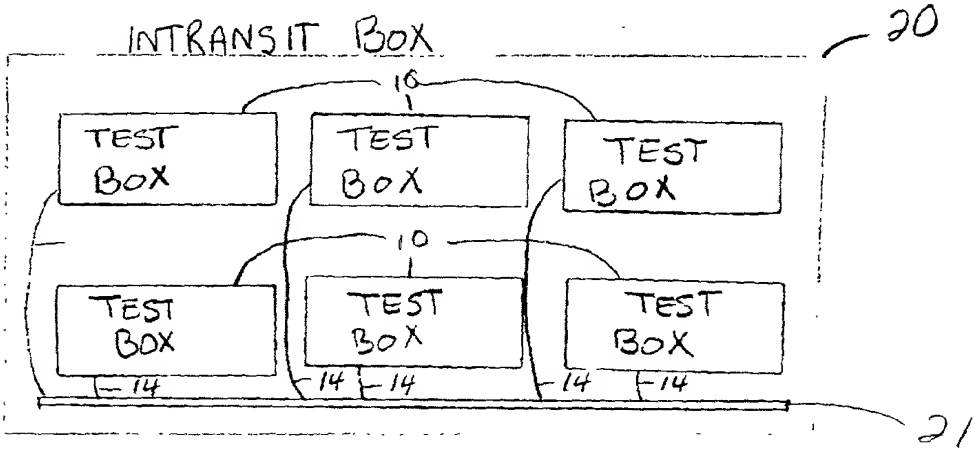

Figure 2

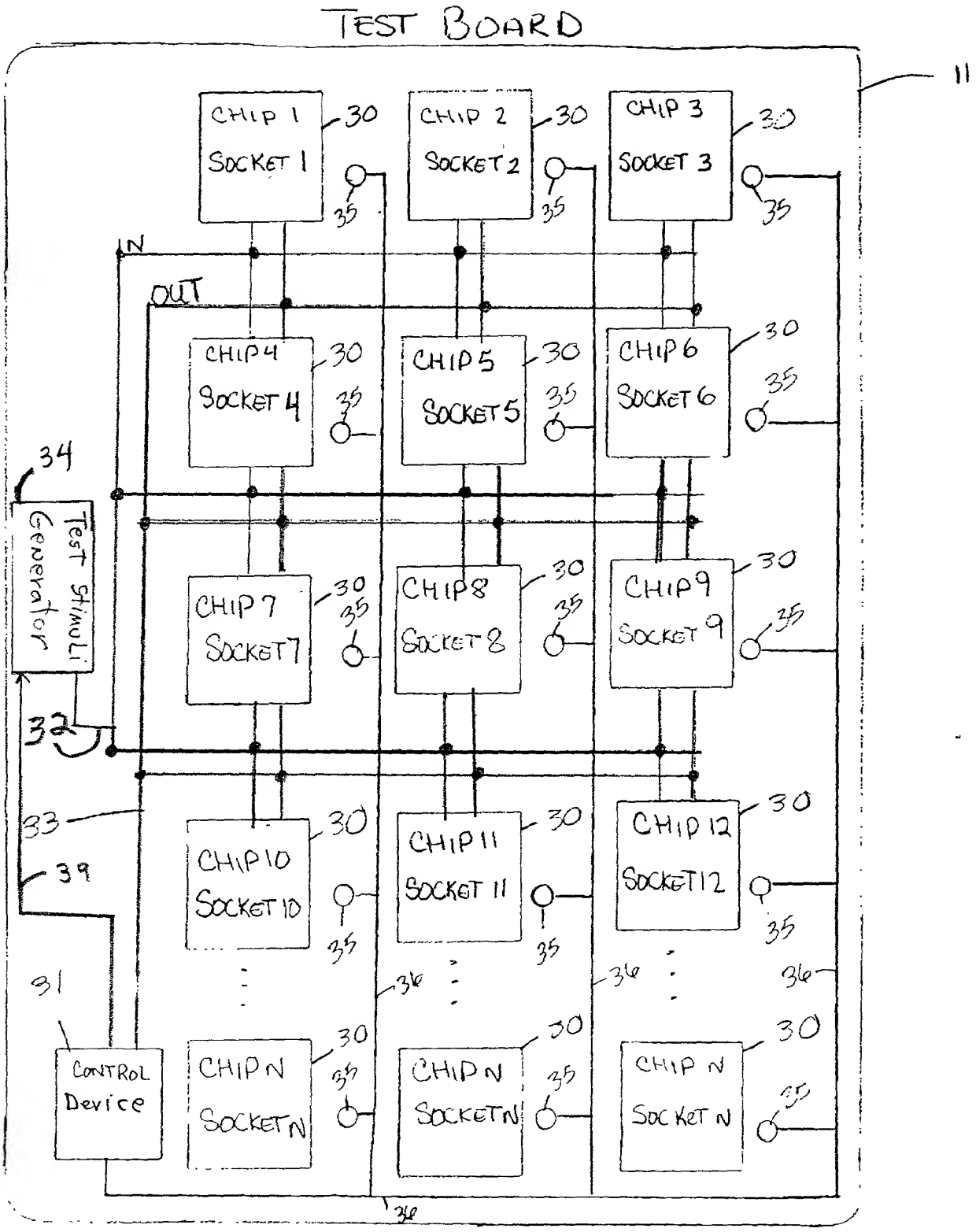
TEST BOARD
11
CHIP 1
SOCKET 1
CHIP 2
SOCKET 2
CHIP 3
SOCKET 3
30
35
IN
OUT
CHIP 4
SOCKET 4
CHIP 5
SOCKET 5
CHIP 6
SOCKET 6
34
Test Stimuli Generator
CHIP 7
SOCKET 7
CHIP 8
SOCKET 8
CHIP 9
SOCKET 9
32
33
39
CHIP 10
SOCKET 10
CHIP 11
SOCKET 11
CHIP 12
SOCKET 12
36
31
CONTROL Device
CHIP N
SOCKET N

Figure 3

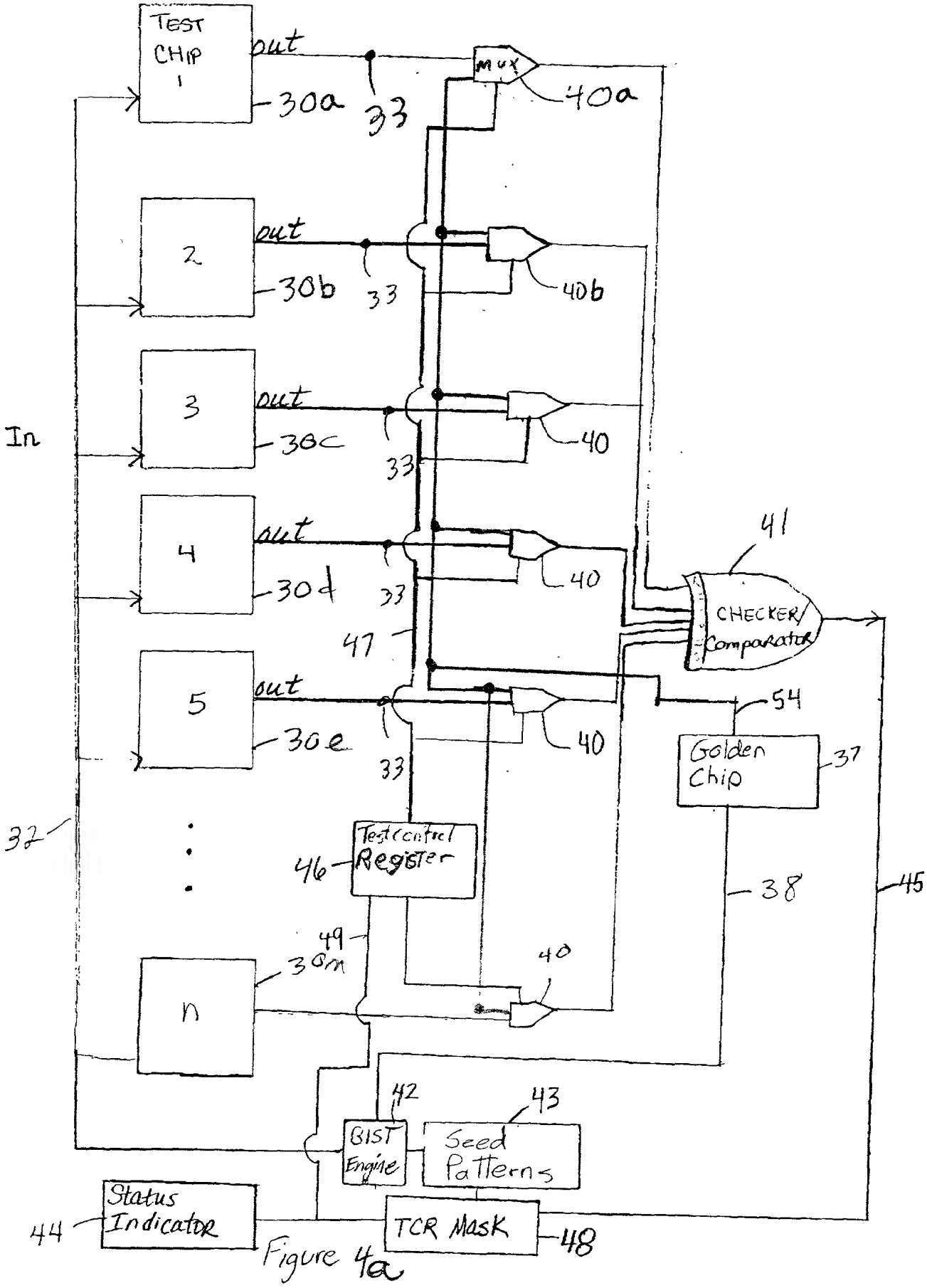
TEST CHIP 1
out
30a
33
MUX
40a
2
out
30b
33
40b
3
out
30c
33
40
In
4
out
30d
33
40
41
CHECKER/ Comparator
47
5
out
30e
33
40
54
Golden Chip
37
32
Test control Register
46
38
45
49
30n
40
n
42
43
BIST Engine
Seed Patterns
Status Indicator
44
TCR Mask
48

Figure 4a

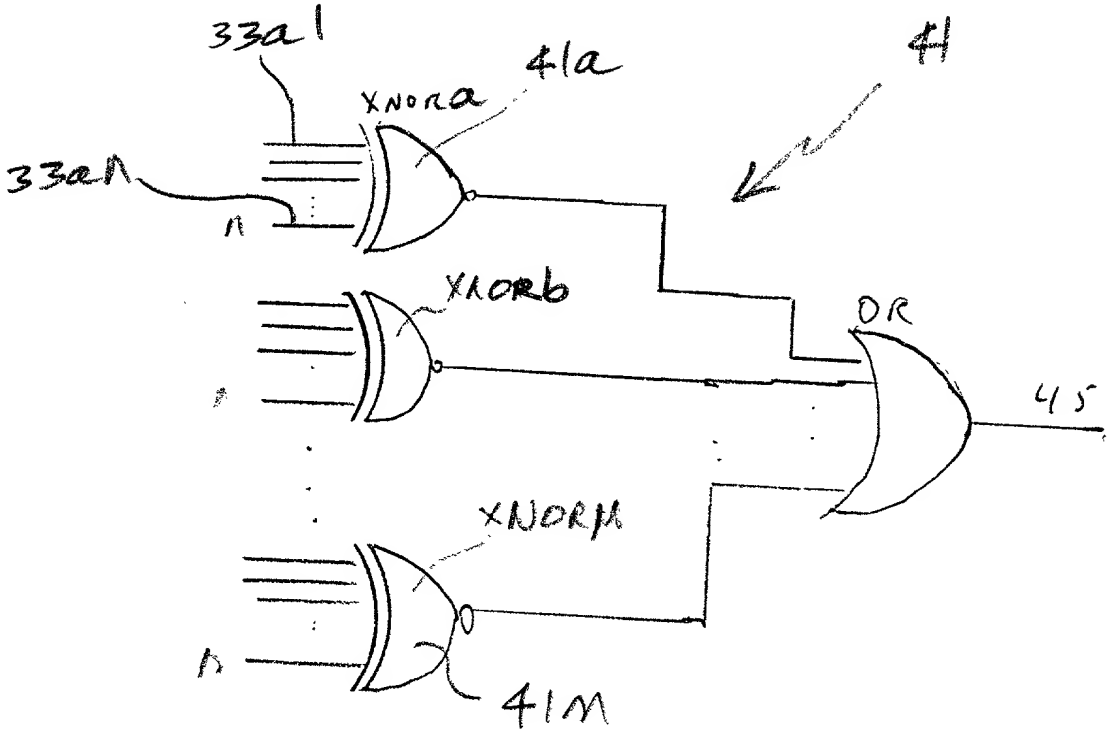

Figure 46: CHECKER/COMPARATOR

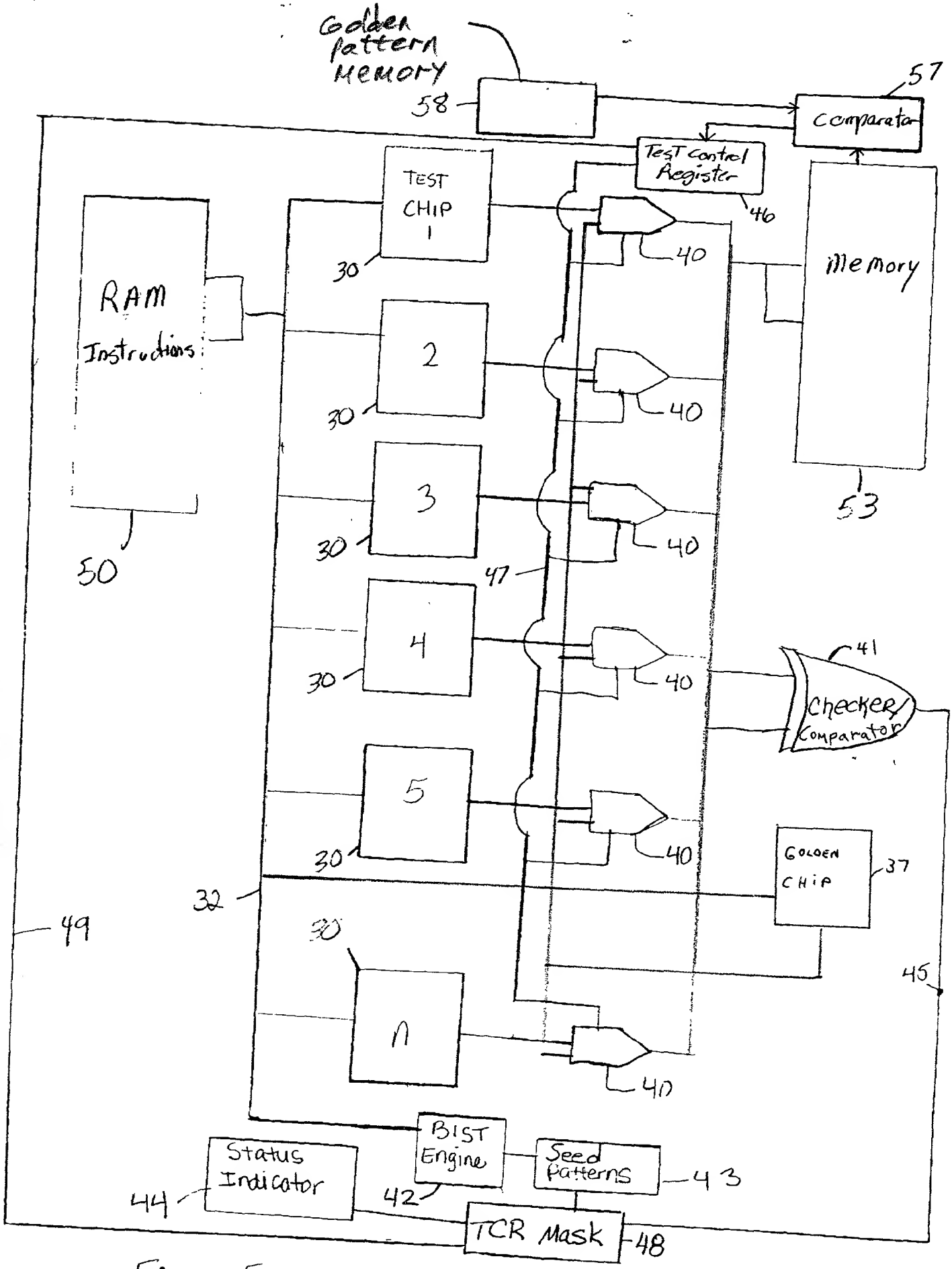
Golden pattern memory
58
57
Comparator
Test Control Register
46
TEST CHIP 1
30
40
RAM
Instructions
50
2
3
4
5
N
47
Memory
53
41
Checker/ Comparator
GOLDEN CHIP
37
32
49
45
BIST Engine
42
Seed Patterns
43
Status Indicator
44
TCR Mask
48

Figure 5

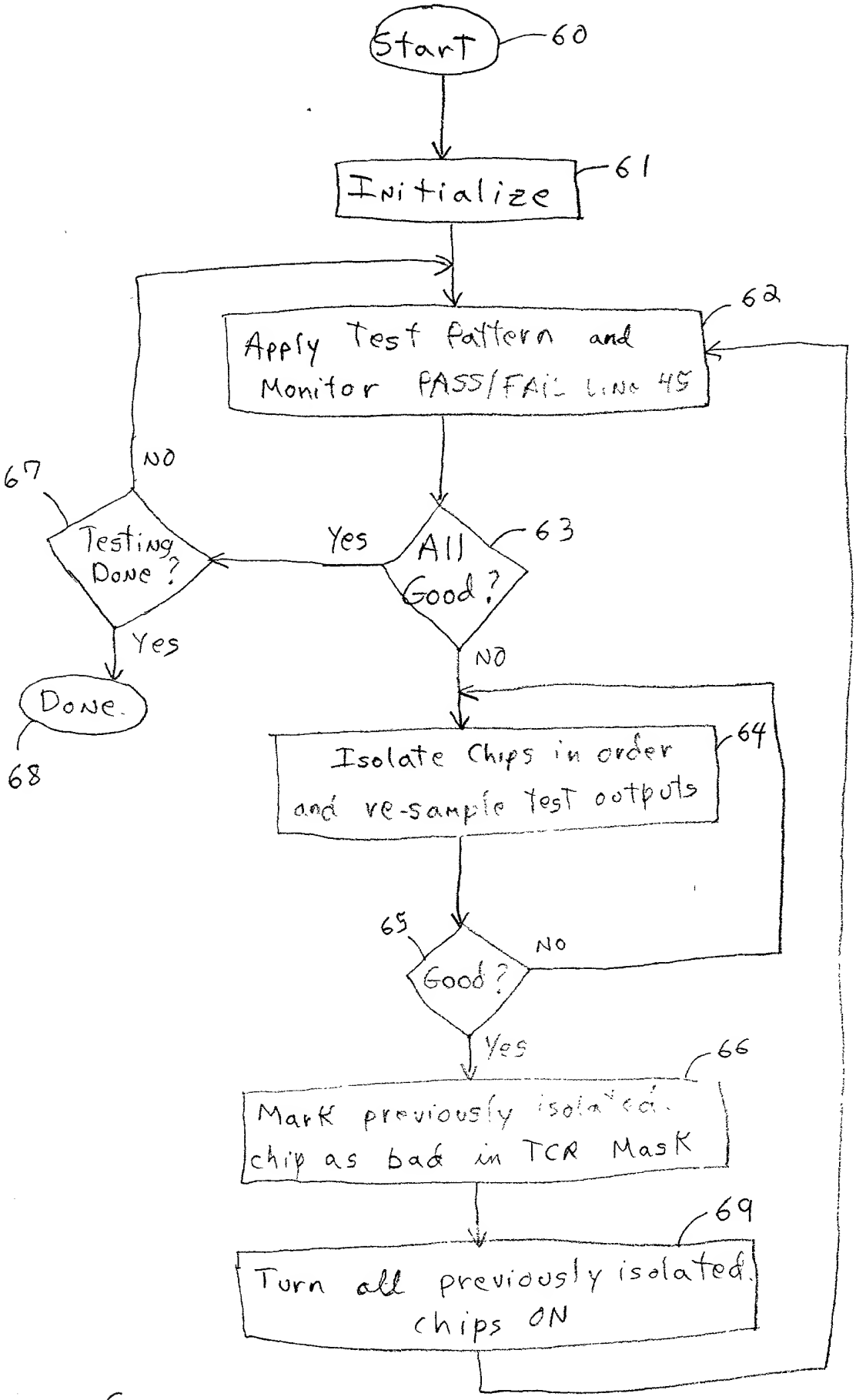
Start
60
Initialize
61
Apply Test Pattern and Monitor PASS/FAIL Line 45
62
All Good?
63
Yes
NO
Testing Done?
67
NO
Yes
Done
68
Isolate Chips in order and re-sample Test outputs
64
Good?
65
NO
Yes
Mark previously isolated chip as bad in TCR Mask
66
Turn all previously isolated chips ON
69

Figure 6.

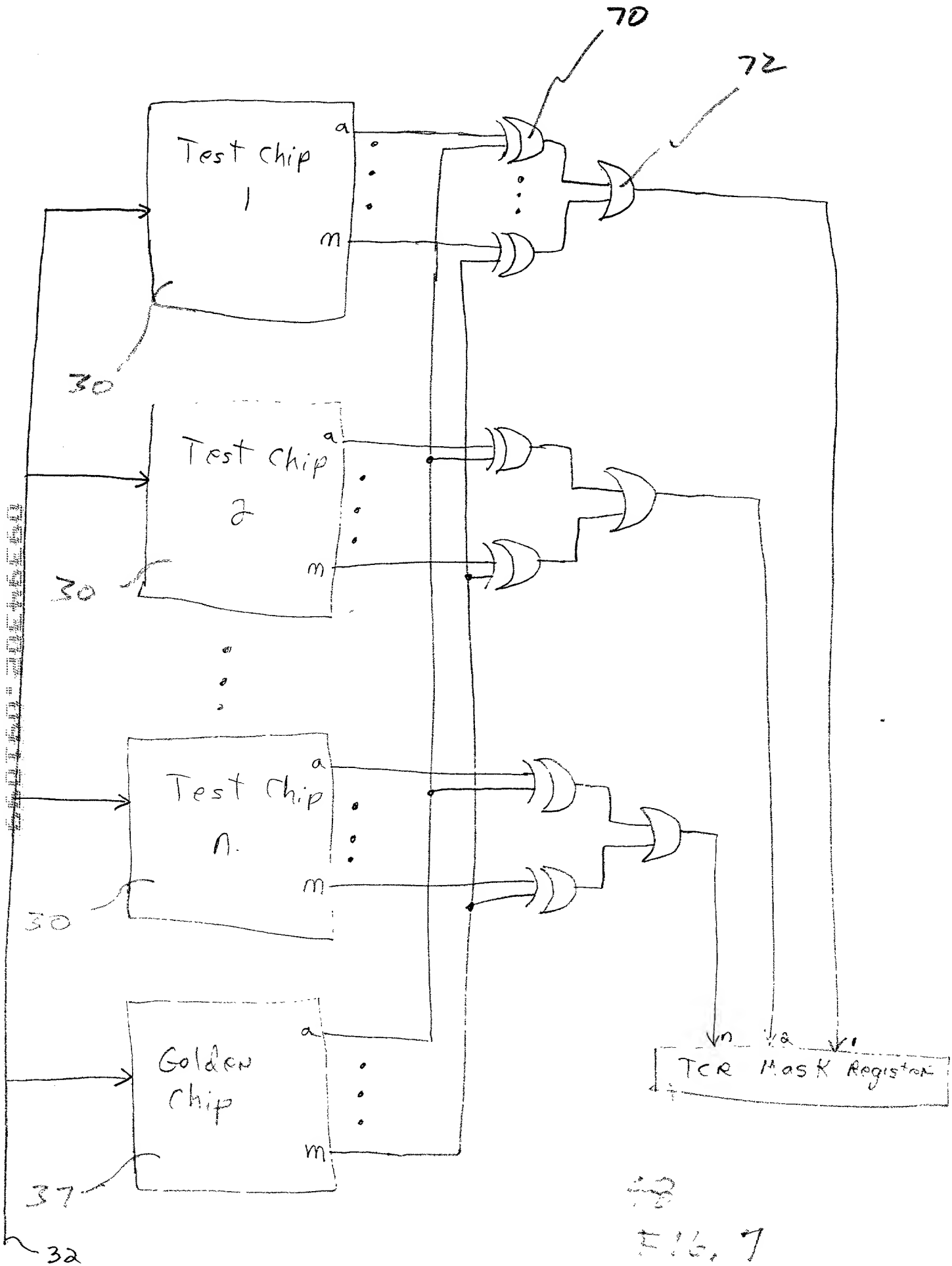
70
72
Test chip 1
a
m
30
Test chip 2
a
m
30
Test chip n.
a
m
30
Golden Chip
a
m
37
32
n
2
1
TCR Mask Register

Fig. 7

Declaration and Power of Attorney for Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: TEST SYSTEM FOR INTEGRATED CIRCUITS

the specification of which (check one)

[X] is attached hereto.

[ ] was filed on _____ as Application Serial No. _____ and was amended on _____

_____.

I hereby state that I have reviewed and understand the contents of the above- identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s).

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications

Serial No.	Filing Date	Status

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: **Mark F. Chadurjian, Reg. No. 30,739; Richard A. Henkler, Reg. No. 39,220; Richard M. Kotulak, Reg. No. 27,712; James M. Leas, Reg. No. 34,372; William D. Sabo, Reg. No. 27,465; Eugene I. Shkurko, Reg. No. 36,678; Robert A. Walsh, Reg. No. 26,516 and Howard J. Walter, Jr., Reg. No. 24,832.**

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